Product Brief
March 2018
Ver. 1.10

DINI Group

DNPCIE_400G_VU_LL

Monsters's Gastrointestinal Disorder

Ethernet Packet Analysis Engine, Latency Optimized | Virtex UltraScale+/UltraScale FPGA PCIe (GEN3/GEN4) card with quad QSFP28 for 100/40/10GbE

Features

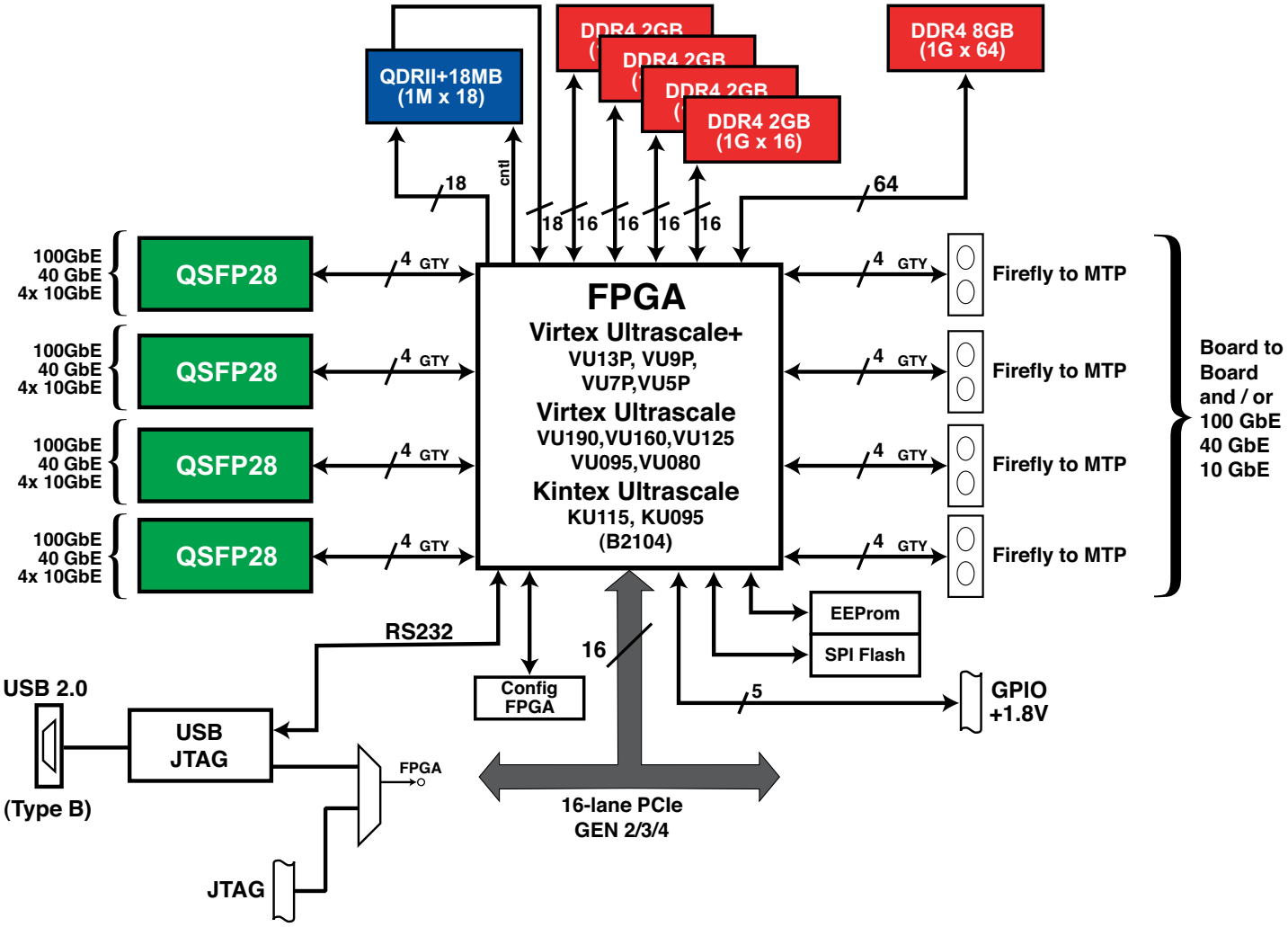
- Quad QSFP28 sockets. Each socket can be:
  - 4-ports 10 GbE or
  - 1-port 40 GbE or
  - 1-port 100 GbE (UltraScale+ only)
- 4 separate Samtec Firefly connectors for MTP
  - 4 GTY lanes per connector
  - Additional 10/40/100GbE ports or board-to-board connections
- Hosted in a 16-lane GEN3/GEN4 PCIe slot (GEN4 with 8-lanes)
  - Compatible with **Xilinx PCI Express Solutions**
  - Compatible with **Northwest Logic PCI Express Solutions**
  - PCIe full, height, GPU length
- Fully compatible with our **optional** **TCP Offload Engine (TOE/TOE128)**
- **Optional** FIX board support package (**DN_FBSP**). Functioning reference design with:
  - 10 GbE/40GbE/100GbE MAC
  - TCP/IP Offload Engine (TOE)
    - Up to 128 sessions
  - FIX protocol parser
  - PCIe Interface (16-lane, GEN3)
  - Memory
    - QRDII+ Controller
    - DDR4 Controller
- Xilinx Virtex UltraScale+/UltraScale FPGA (B2104)
  - Virtex UltraScale+: VU13P, VU11P, VU9P, VU70, VU5P
  - Virtex UltraScale: VU190, VU160 VU125, VU095, VU080
  - Kintex UltraScale: KU115, KU095
- 20M ASIC gates (ASIC measure) when stuffed with VU13P
  - 1.7M flip-flop/6-input LUTs (3.4M total FFs)
  - 58 Mbytes total FPGA block memory
  - 11,904 multipliers: 27 x 18
- DDR4 Memory (16GB total) in 5 separate blocks
  - 4 blocks: 1G x 16
  - 1 block: 1G x 64
  - 1200MHz operation, PC4-2400
  - DDR4 interface compatible with Vivado MIG
- QDRII+ configured as 1M x 18
  - 1200Mb/sec (600MHz)
- SMBus-based thermal management
- 5 bits of 1.8V general purpose I/O (GPIO)
- Full support for embedded logic analyzers via JTAG interface
  - ChipScope Integrated Logic Analyzer (ILA), **Exostiv**, and other third-party debug solutions
- Eight FPGA-controlled LEDs
  - Enough debug LEDs to illuminate virtually nothing.

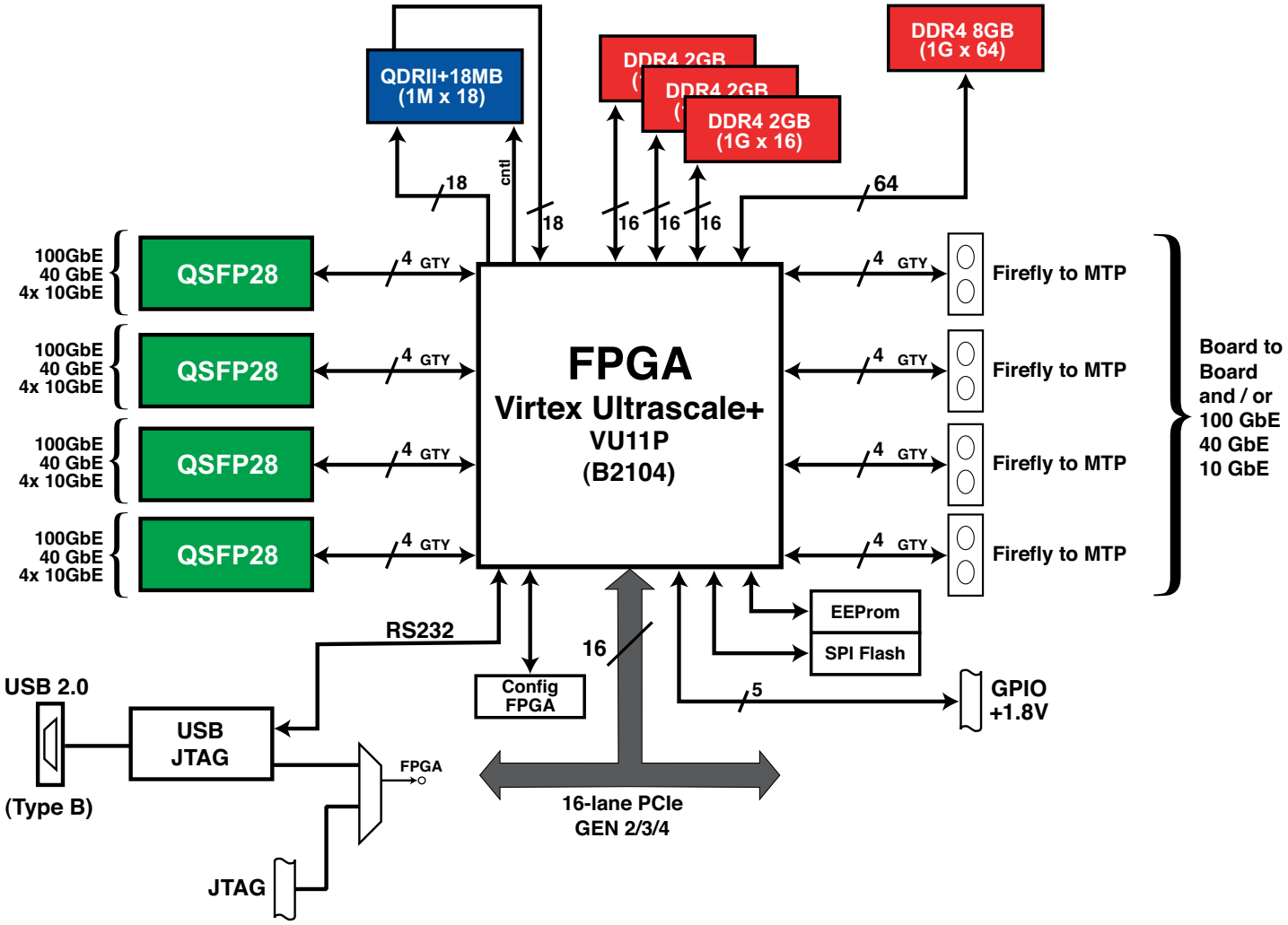
Description

Overview

The **DNPCIE_400G_VU_LL** is a PCIe-based FPGA board designed to minimize input to output processing latency on 10-Gbit, 40-Gbit, or 100GbE Ethernet packets. The primary application is for low-cost, low latency, high throughput trading **without** CPU intervention. Every possible variable that affects input to output latency has been analyzed and minimized. Raw 10/40/100 GbE Ethernet packets can be analyzed and acted upon without a MAC, interrupts, or an operating system adding delay to the process. This configurable hardware computing platform has the ability to achieve the theoretical **minimum** Ethernet packet processing latency.

Block Diagrams




QDRII+18MB
(1M x 18)
DDR4 2GB
DDR4 2GB
DDR4 2GB
(1G x 16)
DDR4 8GB
(1G x 64)
18
cntl
18
16
16
16
64
100GbE
40 GbE
4x 10GbE
QSFP28
4 GTY
FPGA
Virtex Ultrascale+
VU11P
(B2104)
Firefly to MTP
Board to
Board
and / or
100 GbE
40 GbE
10 GbE
EEProm
SPI Flash
RS232
16
Config
FPGA
5
GPIO
+1.8V
USB 2.0
(Type B)
USB
JTAG
FPGA
JTAG
16-lane PCIe
GEN 2/3/4

The FPGA – Xilinx Virtex UltraScale+/UltraScale

We use a single FPGA from the Xilinx Virtex UltraScale+/UltraScale family in the B2104 package. This package supports 702 I/Os with the majority utilized. Most are dedicated to off chip memory peripherals including a single QDRII+ dual port memory and several banks of DDR4 memories. The Virtex UltraScale/ UltraScale+ FPGA contains high-speed transceivers capable of 25 GHz. Sixteen of these transceivers are used for a 16-lane GEN3/4 PCIe interface. Four sets of 4 GTY transceivers are connected to QSFP28 sockets for 40/100GbE Ethernet (or 4 channels of 10 GbE). Sixteen addition GTY transceivers are attached to Samtec Firefly connectors and can be used for high speed board to board communication using cables or more 10/40/100GbE ports

Ten possible UltraScale+/UltraScale FPGAs can be stuffed: VU13P, VU11P, VU9P, VU70, VU5P and VU190, VU160 VU125, VU095, VU080. Two possible Kintex UltraScale FPGAs can be stuffed: KU115, KU095 but note some reduced performance on the GTY interfaces. These FPGAs come in a variety of speed grades (-3, -2E/2I, -1/1L) with -3 the fastest. -2 or faster might is required to achieve the highest clock rates on the memory interfaces. Table 1 depicts the resources of the FPGAs with the Xilinx marketing exaggerations excised. These are large FPGAs, with Kintex being the most cost effective. The VU13P is capable of handling ~20M ASIC gates of logic and remember that the internal FPGA memory and multiplier blocks are not part of this number. UltraScale+ adds large blocks of internal RAM (UltraRAM). Features of the Xilinx UltraScale/UltraScale+ FPGAs include efficient, dual-register 6-input look-up table (LUT) logic, 18 Kb (2 x 9 Kb) block RAMs, and third generation DSP slices (includes 27 x 18 multipliers and 48-bit accumulator). Floating point functions can be implemented using these DSP slices.

Low Latency Network Interface

4 channels of 40/100 GbE or a mix of 10 GbE via quad QSFP28

The Virtex UltraScale/UltraScale+ FPGA has transceivers capable of 25 GbE. The physical interface (PHY) is handled using dual QSFP28 modules for 40/100 GbE. With the proper cable this can be split into 4 separate channels of 10 GbE. Raw Ethernet packets can be accessed directly by bypassing the MAC.

Memory

QDR II+ SSRAM - Memory with the lowest latency

We use a single quad data rate static RAMs (QDR II+ SSRAM) in the 8M x 18 size (144Mbit). This type of memory has separate input and output data paths enabling maximum read/write data bandwidth with minimum latency. The maximum tested frequency of this memory is 550 MHz. To minimize processing latency, we suspect it will be best to clock this QDRII+ SRAM at 312.50 MHz, exactly twice the internal Ethernet controller frequency of 156.25 MHz. The FPGAs are capable of generating internal 2x clocks that are phase synchronous, eliminating the latencies associated with the tricky re-synchronization of data moving between different clock frequencies. The internal controller can be optimized in any way you choose. We, of course, provide several Verilog examples for no charge that you are welcome to use. All functions of the QDR II+ SSRAM can be exploited, including concurrent read and write operations and four-tick bursts. The only real limitation is the amount of time and effort spent in customizing the individual memory controllers.

DDR4 – 16GB of local bulk memory

PC4-2400 DDR4 chips are mounted on the card, providing 5 different banks of DDR4 memory. One bank is configured as 1G x 64. Four additional banks are configured as 1G x 16. **Note that the VU11P loses a single bank of 1G x 16 memory**. Using a -2 or -3 speed grade FPGA, this memory bank is tested at the maximum FPGA I/O frequency: 1200 MHz (2400 Mb/s with DDR).

To minimize data synchronization across clock boundaries, it probably makes sense to clock this DDR4 interface at a 7x multiple of the base Ethernet frequency of 156.25 MHz, which is 1093.75 MHz A 9x phase synchronous clock can be easily generated internal to the FPGA, allowing zero latency synchronous data transfers between the Ethernet packet receiving logic and the DDR4 memory controller. The DDR4 controller can be optimized in any way you choose. We, of course, provide several Verilog examples for no charge that you are welcome to use. All functions of the DDR4 DRAM can be exploited and optimized. Up to 8 banks can be open at once. Timing variables such as CAS latency and precharge can be tailored to the minimum given your operating frequency and the timing specification of the exact DDR4 memory utilized. As with the QDRII+, the only real limitation is the amount of time and effort spent customizing the DDR4 memory controller to your needs.

PCIe – Customizable 16-lane, GEN3/4 PCI Express

PCIe is connected directly to the FPGA via 16-lanes of GTY transceivers. The interface is fully GEN2/GEN3 and GEN4 capable. We ship GEN3 PCIe IP that is a full function, fixed, 16-lane master/target. To gain access to the PCIe interface, this IP must be integrated with your application. The Dini Group PCIe IP provides a flexible interface that allows the user access to multiple DMA engines, scratchpad memories, interrupts, and other endpoint-related functions to maximize performance while utilizing minimal FPGA resources. Drivers (required) for ‘C’ source for several operating systems are included no charge.

How Everything Works ….

With direct data feeds such as NASDAQ ITCH and OUCH, the **DNPCIE_400G_VU_LL** contains all of the basic functions required to minimize the amount of time it takes to receive Ethernet packets, process them, and respond deterministically. By using the FPGA to process Ethernet packets, the processor and operating system are removed from the critical path and traditional sources of latency such as interrupts and context switching no longer hinder performance. Not a single clock cycle is wasted. For algorithms requiring processing, FPGA resources can be hard coded to perform the task. This includes real-time Monte Carlo analysis, and floating point.

UltraScale+		Speed Grades (slowest to fastest)	FF's	Gate Estimate		Multipliers (27x18)	Memory			
				Max (100% util) (1000's)	Practical (60% util) (1000's)		Blocks UltraRAM (4k x 72bits)	Block RAM (18kbits)	Total (kbits)	Total (kbytes)
Virtex	VU13P	-1,-2,-3	3,456,000	33,178	19,910	11,904	1,280	5,376	465,408	58,176
	VU11P	-1,-2,-3	2,592,000	24,883	14,930	8,928	960	4,032	349,056	43,632
	VU9P	-1,-2,-3	2,364,480	22,699	13,620	6,840	960	4,320	354,240	44,280
	VU7P	-1,-2,-3	1,576,320	15,133	9,080	4,560	640	2,880	236,160	29,520
	VU5P	-1,-2,-3	1,201,154	11,531	6,920	3,474	470	2,048	172,224	21,528

UltraScale		Speed Grades (slowest to fastest)	FF's	Gate Estimate		Multipliers (27x18)	Memory		
				Max (100% util) (1000's)	Practical (60% util) (1000's)		Blocks (18kbits)	Total (kbits)	Total (kbytes)
Virtex	VU190	-1,-2,-3	2,148,480	20,625	12,380	1,800	7,560	136,080	17,010
	VU160	-1,-2,-3	1,852,800	17,787	10,670	1,560	6,552	117,936	14,742
	VU125	-1,-2,-3	1,432,320	13,750	8,250	1,200	5,040	90,720	11,340
	VU095	-1,-2,-3	1,075,200	10,322	6,190	768	3,456	62,208	7,776
	VU080	-1,-2,-3	891,429	8,558	5,130	672	2,842	51,156	6,395
Kintex	KU115	-1,-2,-3	1,326,720	12,737	7,640	5,520	4,320	77,760	9,720
	KU095	-1,-2	1,075,200	10,322	6,190	768	3,360	60,480	7,560

For technical applications and sales support, call 858.454.3419

DINI Group

7469 Draper Ave.
La Jolla, CA 92037-5026
Phone: 858.454.3419
Fax: 858.454.1728
E-Mail: sales@dinigroup.com
Web: http://www.dinigroup.com

The DINI Group reserves the right to make changes to the product(s) or information contained herein without notice. No liability is assumed as a result of their use or application. No rights under any patent accompany the sale of any such product(s) or information.