# SmartDV™

***The Leader in IP Technology and Support***

## SmartDV Announces OpenCAPI™ Verification IP (VIP)

*Partnered with Major Corporation to Develop a Fully Functional VIP*

**San Jose, CA – April 24, 2018** – SmartDV announces today that it has joined the OpenCAPI Consortium, an open development community based on Coherent Accelerator Processor Interface technology. Upon joining, SmartDV is also announcing today the delivery of an OpenCAPI VIP.

SmartDV joins a growing roster of technology organizations that are contributing to the OpenCAPI Consortium and driving data center server innovation. Through the Consortium, members are working collaboratively to innovate on top of OpenCAPI, a high performance coherent bus standard designed to help the technology industry meet growing demands for more advanced memory, accelerators, networking and storage technology. Using the OpenCAPI specification, developers can enable high performance accelerators like FPGAs, GPUs, network and storage accelerators to perform functions that a server's general purpose CPU is not optimized to execute. Because OpenCAPI technology has been made available to the entire industry through the Consortium, SmartDV has embraced open collaboration with other industry leaders to enable innovation and differentiated products to be brought to market faster.

The SmartDV OpenCAPI Verification IP is fully functional and shipping today. Deepak Kumar Tala, Managing Director of SmartDV Technologies India Private Limited said: "we have been working with one of our major customers, who is also an OpenCAPI member, to develop and verify our OpenCAPI Verification IP product. We are working closely with the Consortium and will deliver additional products to support the standard."

"The development model of the OpenCAPI Consortium is one that elicits collaboration and represents a new way in exploiting and innovating around coherent accelerator processor technology," says Scott Graham, OpenCAPI Consortium Chair. "New OpenCAPI Consortium members like SmartDV will be able to create and add their own innovations to further advance differentiation and growth of the OpenCAPI ecosystem."

**About OpenCAPI**
To learn more about OpenCAPI and to view the complete list of current members, go to www.opencapi.org.

**About SmartDV**
SmartDV was founded in 2008 by three senior engineers with extensive experience in the design and verification of complex ASICs. SmartDV has a staff of over 200 engineer focused on semiconductor design and VIP. SmartDV maintains its IP leadership position by continuously staying atop the latest technology advances and bringing that information to its customers. Our of the company's strengths is the SmartCompiler™ technology that automates the consistent generation of IP and the writing of the verification environment and test cases for ASIC verification, significantly saving ASIC verification time.

SmartDV offers high quality standard and custom protocol Verification IP, Memory Models, Simulation Acceleration (Emulation) IP and Design IP covering MIPI, Networking, Video, Storage, Automotive and processor interfaces. The VIP and Design IP are licensed to over 120 world-wide customers including the industry's leading semiconductor and system companies. SmartDV also offers ASIC and FPGA design and verification services with an emphasis on quality deliverables. SmartDV VIP are 2-4x faster to compile and simulate compared to our competition.

SmartDV is headquartered in Bangalore, India with local offices in San Jose, CA. More information can be found at www.smart-dv.com.

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